REMARKS

The premise of the Examiner's position seems to be that because two references teach using a single integrated circuit with isolation devices in between regions thereof, that somehow the combination of these two references teaches using separate integrated circuits. An assertion of equivalency is not sufficient to meet the claimed invention. It does not matter whether the two circuits are functional equivalents. What matters is whether or not anything teaches what is claimed.

As explained in the Background of the present application at page 2, line 15, existing modems generally are implemented using two or more integrated circuits. One set of integrated circuits provides most of the digital signal processing and the other provides the analog to digital and digital to analog conversion. Generally, the two integrated circuits are separated after A to D conversion on the receiver side and before D to A conversion on the transmitter side. This means that data is transmitted between the two chips at relatively high data rates. This high data rate transmission results in more buffering on each chip and more pins are needed to connect the chips. This increases the cost of each chip. In addition, the high data rate results in higher system cost due to the impact of higher frequency operation and electromagnetic interference shielding.

Thus, the problem that was sought to be overcome is the one of using two separate integrated circuits, but transmitting the data between them at high data rates.

Nothing in any of the cited references suggest slowing down the data rate before transferring the data between two spaced integrated circuits. This failure of teaching makes the rejection insufficient to make out a *prima facie* rejection. Nothing has addressed the problem solved by the claimed invention. Neither of the two cited references are even faced with the same problem.

Both of the two references use a single integrated circuit as plainly depicted in their figures. The fact that they, according to the Examiner, contemplated having isolating capacitors that are separate integrated circuits is noted, but, there is no transmission between two separate integrated circuits in any of the cited references.

More poignantly, if one were to accept the Examiner's proposition that the Kanekawa reference could be effectively considered to be split in two by virtual of the circuit elements 50 and 2, along a vertical line in Figure 23, the Examiner has then presented a reference which

constitutes the prior art whose problems the present invention sought to overcome. In other words, the reference shown in Figure 23 is not even as close to the present invention as what was already discussed in the Background. If one were to modify that reference with no teaching in the prior art, to make two separate circuits, all one would have would be exactly the circuit that had the very problems set forth in the Background.

The Examiner points to another reference which still does not use separate integrated circuits. Neither reference teaches a solution to the problems arising from data transfer between separate chips.

Since Yakutake used a single integrated circuit, there is nothing in Yakutake that would suggest the solution to the problems faced when separate integrated circuits are used. Whatever reason Yakutake had for decimating the data had nothing to do with the problems that arise when separate integrated circuits are provided. That is necessarily so because Yakutake did not have separate integrated circuits.

Thus, if one were to modify Kanekawa as proposed by the Examiner, he would then face all of the deficiencies noted in the Background. It seems illogical to suggest that he would appreciate the solution to those problems in a reference that does not even use two separate circuits and, therefore, does not even solve the problems.

This is merely hindsight reasoning. It is the suggestion that decimation could be used to overcome problems because a reference teaches decimation for some other purpose. There is no suggestion of using the decimation before transferring the data from one integrated circuit to another. Therefore, the fact that decimation is used before data is transferred across regions of the same integrated circuit simply does not teach a solution to the problems solved by the present invention and faced by Kanekawa.

In short, there is no teaching in any of the references or their combination of a solution to the problem only recognized by the present applicants. Therefore, reconsideration is requested.

Respectfully submitted,

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Timothy N. Trop, Reg. No. 28,994
TROP, PRUNER & HU, P.C.
8554 Katy Freeway, Suite 100
Houston, Texas 77024
(713) 468-8880 [Phone]
(713) 468-8883 [Fax]

Attorneys for Intel Corporation